REMARKS

Claims 41-67 are pending in the present application. In the office action mailed October 9, 2003 (the "Office Action"), claims 41-43, 45-48, and 54-64 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,134,681 to Akamatsu *et al.* (the "Akamatsu patent") in view of Hancu *et al.*, "A Concurrent Test Architecture For Massively Parallel Computers and Its Error Detection Capability," IEEE Transactions on Parallel and Distributed Systems, pp. 1169-84, Vol. 5, Issue 11 (the "Hancu article"). Claims 44, 49-53, and 65-67 were rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of the Akamatsu patent in view of the Hancu article. More specifically, in further view of U.S. Patent No. 4,642,793 to Meaden (the "Meaden patent"), or in further view of U.S. Patent No. 5,659,737 to Matsuda (the "Matsuda patent"), or in further view of IBM technical disclosure bulletin entitled, Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory, June 1, 1988 (the "IBM technical disclosure").

The Examiner has characterized the Akamatsu patent as teaching "the procedure for the claimed method of accessing a memory via test instructions or commands, means to initiate test mode, comprising: comparing memory addresses for a fault memory analysis (access/test) by performing substitute address allocation (mapping or remapping) and provides compression means in col. 2 lines 35-50 . . . ." *See* the Office Action at page 1. The Examiner further cites to the Hancu article for teaching address compressing in memory testing because the Akamatsu patent does not describe, "whereby compressing is effected on addresses as a means for reducing failure storage hardware." *See id.* at page 2.

The Akamatsu patent describes a memory device that includes a fuse circuit and a signal generation circuit that allows column selection in the memory device to occur sooner than in a conventional memory device, in the situation where none of the redundant memory locations (*i.e.*, redundant rows and columns of memory) for a memory array have been used. The problem with conventional memory devices, as described in the Akamatsu patent, is that column selection begins only after a certain time following the latching of the column addresses by the memory device (in response to a column address transition), regardless of whether any redundant memory needs to be accessed. *See* Figure 17. Based on the conventional design of the fuse circuit and the signal generation circuit, if the memory access operation is begun before the minimum time

elapses, such as immediately after a transition in the column address is detected, and it is later determined that a redundant column memory should be accessed instead of the actual column of memory, the selection of multiple columns will occur.

The memory device described in the Akamatsu patent includes a fuse circuit 1 and a signal generation circuit 10, shown in Figures 1 and 2, respectively, such that multi-selection of columns is avoided, but in the event none of the redundant columns of memory are used for an array, selection of the column for access can begin sooner than if redundant columns of memory have been used in the memory array. The benefit in timing resulting from the fuse circuit 1 and signal generation circuit 10 is illustrated with respect to Figure 4. Alternative embodiments of the signal generation circuit are described in the Akamatsu patent as well, each having different types of delay circuits. *See* Figures 5-7.

The material in the Akamatsu patent cited by the Examiner, namely, col. 2, lines 35-50, is found in the Background of the Invention. The cited material generally describes a memory access operation, with specific reference to activating a row and a column of memory cells in a memory array. Although a "compression means" is purportedly described in the Akamatsu patent, *see* the Office Action at page 1, there is no mention of any type of compression or compression means in the cited material. In fact, after reviewing the *entire* patent, the term "compression" is not once mentioned. In the event that the rejections to the claims are maintained, the Examiner is requested to cite the particular material in which a "compression means" is described in the Akamatsu patent.

The Hancu article, as previously described in the response to office action filed July 24, 2003, describes a method for testing multiprocessor systems. Signature analyzers ("SAs") are included in the network of a multiprocessor system to monitor devices at every node of the network. Packets having source addresses, destination addresses, and data are routed through the network in order to track control flow of the packets. At the end of the routing process, the signatures of the packets are compared against pre-calculated reference values in order to determine whether the packet arrived at a destination following the correct route. Additionally, the contents of the SAs are also compared against reference values to determine if an algorithm is executed correctly. The address compression performed by the SAs takes a

source and destination address and provides a value that is passed to subsequent SAs in the program path until arriving at a destination for comparison to a reference signature.

As previously mentioned, claims 41-43, 45-48, and 54-64 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Akamatsu patent in view of the Hancu article. The rejection of claims 41, 45, 54, and 59 as being unpatentable over the Akamatsu patent in view of the Hancu article cannot be maintained. A first reason is that those ordinarily skilled in the art would not have been motivated to combine the teachings of the Akamatsu patent and the Hancu article. A second reason is that even if the teachings of the Akamatsu patent were combined with the teachings of the Hancu article, the combined teachings fail to teach or suggest the combination of limitations recited in claim 41.

As previously discussed, the Akamatsu patent is directed to a memory device including fuse and signal generation circuits that allow access to a column of memory to occur sooner than otherwise when no redundant columns of memory are used for a memory array. The Akamatsu patent is directed to column address decoding and the activation of a column of memory, redundant or actual. Moreover, despite the Examiner's assertion to the otherwise, there is no discussion of compression anywhere in the Akamatsu patent. The Hancu article is directed to testing a multiprocessor system. Address compression is used in establishing the run-time signature of the system in order to monitor data dependencies and control flow of packets in the network. It is unlikely that one ordinarily skilled in the art would be motivated to combine the teachings of the Akamatsu patent and the Hancu article since the "address compression" relied upon by the Examiner is inapplicable to the memory device described in the Akamatsu patent. For the memory device described therein, the addresses that are mapped to redundant memory are stored in a fixed number of fuses or antifuses, as is conventional. The address compression described in the Hancu article is algorithmic, that is, calculating a new value from a received value. If the memory addresses are stored in a read-only medium that cannot be modified in value or length, such as storing the addresses using fuses or antifuses, it is doubtful that a compression algorithm as used in the multiprocessor testing method described in the Hancu article would be combined with the memory device described in the Akamatsu patent.

Additionally, it makes no sense to apply the testing method using packet routing for testing a multiprocessor system, as described in the Hancu article, to a memory device having

the fuse and signal generating circuits described in the Akamatsu patent. Even at the most general level, the use of address compression described in the Hancu article has nothing to do with the memory device described in the Akamatsu patent. For example, packets of information as described in the Hancu article are not routed within a memory device having the fuse circuit and signal generation circuit described in the Akamatsu patent. SAs that are positioned at network nodes in the Hancu article could not be placed in the memory device as well. The two references cited by the Examiner are completely unrelated, in purpose, in subject matter, and in application. Consequently, the Examiner has failed to establish that one of ordinary skill in the art would be motivated to combine the teachings of the Hancu article with the teachings of the Akamatsu patent.

Additionally, even if it were possible to combine the teachings of the two references, the combination would fail to teach or suggest the combination of limitations recited by claims 41, 45, 54, and 59. Claim 41 recites a method for accessing a memory, comprising comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format, the defective memory addresses having substitute addresses associated and stored therewith, where the memory address matches one of the decompressed defective memory addresses, extracting the substitute address associated therewith, and accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address.

Claim 45 recites a method for accessing a memory device receiving memory addresses, the method comprising comparing the received memory addresses to decompressed addresses of defective memory locations in the memory device, the decompressed addresses of the defective memory locations otherwise stored in a compressed format having associated therewith substitute addresses corresponding to substitute memory locations in another memory, and substituting for the memory addresses matching the decompressed addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory.

Claim 54 recites a method for storing memory addresses of defective cells in a memory array, the method comprising receiving a memory test command, initiating a memory test in response to the memory test command, the memory test for determining memory

addresses of defective memory cells of the memory array, mapping memory addresses of defective memory cells to substitute addresses of substitute memory cells, and compressing the memory addresses of defective memory cells and the substitute addresses associated therewith.

Claim 59 recites a method of remapping defective memory locations of a primary memory, the method comprising identifying memory addresses of the defective memory locations in the primary memory, mapping the identified memory addresses of the primary memory to substitute memory addresses that correspond to substitute memory locations in a spare memory, storing the identified memory addresses of the primary memory and the substitute memory addresses of the spare memory, and in response to a request to access a defective memory location in the primary memory, substituting the associated substitute memory address in the spare memory for the memory address corresponding to the requested defective memory location in the primary memory.

Neither the Akamatsu patent nor Hancu article discloses comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format. The extraction of a substitute address associated with the decompressed defective memory address when there is an address match is nowhere to be found in the Akamatsu patent or the Hancu article either. The invocation of a test mode is also not discussed in either reference. The Akamatsu patent and the Hancu article further fail to teach or suggest storing the identified memory addresses of a primary memory and a substitute memory addresses of a spare memory. Based on the previous discussion, on one hand we have a memory device that includes a fuse circuit and a signal generator circuit that allows a shorter delay in selecting a row when none of the redundant columns of memory are used for an array, and on the other hand, we have a method for testing a multiprocessor system where address compression is used as part of establishing a signature of a packet route in order to compare it with a reference signature. The Akamatsu fails to mention anything about address compression. It further fails to mention any test modes. The Hancu article is directed to testing a multiprocessor system, mentioning address compression with respect to the packets routed through the network that is inoperable with the memory device described in the Akamatsu patent. There is nothing in either the Akamatsu patent or the Hancu article that would suggest the combination of limitations recited by claims 41, 45, 54, or 59.

For the foregoing reasons, claims 41, 45, 54, and 59 are patentable over the Akamatsu patent in view of the Hancu article, and therefore, the rejection of claims 41, 45, 54, and 59 under 35 U.S.C. 103(a) should be withdrawn.

Claims 42 and 43, which depend from claim 41, claims 46-48, which depend from claim 45, claims 55-58, which depend from claim 54, and claims 60-63, which depend from claim 59, are also patentable over the Akamatsu patent in view of the Hancu article based on their dependency from a respective allowable base claim. Moreover, the dependent claims add limitations themselves that are not described in either the Akamatsu patent or the Hancu article. For example, claim 46 recites that the decompressed addresses of defective memory locations in the memory device, which are recited in claim 45, stored in a compressed format and wherein comparing the received memory addresses comprises decompressing at least one of the stored addresses of defective memory locations, and comparing a received memory address to the decompressed address. Since the Akamatsu patent does not mention any type of compression, the limitation is clearly not disclosed therein. As for the Hancu article, which is directed to testing a multiprocessor system, defective memory locations are not discussed, compression of addresses for the defective memory locations is not discussed, and comparison of a decompressed memory address with a received address is not discussed. Similarly, claim 60 recites that the primary memory having the defective memory locations, recited in claim 59, comprises a first memory device and the spare memory comprises a second memory device. The Akamatsu article stores the addresses of the defective memory locations using fuses. The Hancu article does not even contemplate storing addresses of defective memory locations. Nowhere is there a discussion of having the addresses for defective memory locations of a first memory device stored in a second memory device.

For the foregoing reasons, claims 42, 43, 46-48, 55-58, and 60-63 are patentable over the Akamatsu patent in view of the Hancu article. Therefore, the rejection of claims 42, 43, 46-48, 55-58, and 60-63 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 44, 49-53, and 65-67 were rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of the Akamatsu patent in view of the Hancu article. More specifically, claims 44, 49-53, and 65-67 were rejected under

the Akamatsu patent in view of the Hancu article, in further view of the Meaden patent, or in further view of the Matsuda patent, or in further view of the IBM technical disclosure.

None of the references cited by the Examiner, namely the Meaden and Matsuda patents, and the IBM technical disclosure, make up for the deficiencies of the Akamatsu patent and the Hancu article, as previously discussed with respect to claims 41-43, 45-48, 54-58, and 59-63. Even if the Examiner's characterizations of the Meaden and Matsuda patents, and the IBM technical disclosure are accurate, the combination of limitations recited by claims 44, 49-53, and 65-67 is neither taught nor suggested by the combined teachings. Additionally, the motivation to combine the Meaden or Matsuda patent, or the IBM technical disclosure with the teachings of the Akamatsu patent and the Hancu article is even further off the mark than the lack of motivation previously discussed with respect to combining the teachings of only the Akamatsu patent and the Hancu article. None of the techniques described in the Meaden and Matsuda patents, and the IBM technical disclosure are applicable to the memory device of the Akamatsu patent or the test method of the Hancu article. Consequently, in addition to the fact the combined teachings of the references fail to teach or suggest the combination of limitations recited by claims 44, 49-53, and 65-67, one ordinarily skilled in the art would not be motivated to combine any of the references in the first place.

For the foregoing reasons, claims 44, 49-53, and 65-67 are patentable over the Akamatsu patent in view of the Hancu article, in further view of either the Meaden or Matsuda patents, or the IBM technical disclosure. Therefore, the rejection of claims 44, 49-53, and 65-67 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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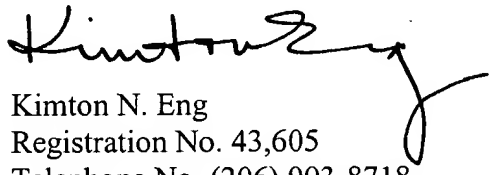

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